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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,552	04/02/2004	Mirsaid Bolorforosh	2004P03346US	2523

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Intellectual Property Department
170 Wood Avenue South
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EXAMINER	
KITOV, ZEEV V	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,552	BOLORFOROSH ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 - 7, 9 - 16, 18 - 21* is/are rejected.

7)☒ Claim(s) *8 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the arguments filed on February 8, 2007. Applicant's Arguments have been given careful consideration but they have been found non-convincing. The Office Action follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 - 6, 12, 13, 15, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. (US 2004/0113524) in view of Shen (US 5,536,958) and Amano (US 7,032,454). Regarding Claims 1, 12 and 20, Baumgartner et al. disclose the capacitive membrane ultrasound transducer (Fig. 1) including a flexible membrane (8 and 12 in Fig. 1) adjacent a void (20 in Fig. 1). It inherently includes a conductor connected with the flexible membrane, since otherwise the transducer cannot function. However, it does not disclose a voltage limiting circuit. Amano teaches that the capacitive membrane is vulnerable to the high voltages (ESD prone, col. 1, lines 62 – 64). Therefore, one of ordinary skill in the art would realize necessity of protecting the capacitive membranes against over-voltages.

Shen discloses the circuit protecting the capacitive gate to substrate structure of the transistor against over-voltages. The voltage limiting circuits (25 and 29 in Fig. 4) protect the capacitive gate to substrate structure of the transistor. The reference is pertinent to the problem solved by the inventor and has the same problem solving area, i.e. protection the capacitive structure vulnerable to ESD against over-voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the voltage limiting circuit connected to the output transducer conductor, because according to Amano (col. 1, lines 62 – 64), the capacitive transducers are vulnerable to the ESD and therefore, need the over-voltage protection.

Regarding Claim 12, Baumgartner et al. disclose the membrane generating either acoustic or electric signal (paragraphs [0002] - [0007]).

Regarding Claim 2, Baumgartner et al. disclose the conductor including an electrode on the flexible membrane (12 in Fig. 1) and inherently a signal trace connected with the electrode, since otherwise the device is inoperative. Since the electrode is located on the top of the flexible membrane an alternative way, i.e. connecting the electrode by any other structure, such as a common ground plate is impossible.

Regarding Claim 3, Shen et al. disclose at least one zener diode connected across the protected device, between the conductor (connected to the gate) and the common electrode. According to Wikipedia (page 21), in an electrical circuit operating at signal voltages (usually less than 50 V or so), a common return path that is the zero

voltage reference level for the equipment or system. Accordingly, The term "ground" is understood as a terminal carrying a common, i.e. reference voltage. Additionally, the grounding symbol used in the Drawings indicates a signal ground, i.e. a common return path that is zero voltage reference for plurality of devices. In Baumgartner et al. system modified according to teachings of Shen et al., the zener diode is connected between the conductor and the substrate (4 in Fig. 1), which is the common return path electrode, i.e. ground. A motivation for modification of the primary reference is the same as above.

Regarding Claim 13, Shen et al. disclose the protection circuits (25 and 29 in Fig. 4) holding a voltage between electrodes constant when the voltage exceeds the preset breakdown voltage. In Baumgartner et al. system modified according to teachings of Shen et al. the breakdown voltage of the zener couple is lower than the breakdown voltage of the membrane. A motivation for modification of the primary reference is the same as above.

Regarding Claim 4 and 15, Shen et al. disclose the protection circuits including two zener diodes in series with opposite polarities (25 and 29 in Fig. 4). A motivation for modification of the primary reference is the same as above.

Regarding Claim 5, Shen et al. disclose a first voltage source and a second voltage source (24 and 27 in Fig. 4). It further discloses a first couple of diodes (25 in Fig. 4) connected between the input terminal and the first voltage reference source (ground) and a second couple of diodes connected between the input terminal and the

second voltage source. A motivation for modification of the primary reference is the same as above.

Regarding Claim 6, the positive and the negative voltage sources are interpreted as positive and negative terminals of the power supply. Shen et al. implicitly discloses the circuit, which for operation is inherently connected to the power supply having positive and negative terminals. A motivation for modification of the primary reference is the same as above.

Regarding Claim 16, Shen et al. disclose limiting the voltage with a first voltage source (27 in Fig. 4) and a first diode (29 in Fig. 4) connected between the input terminal (26 in Fig. 4) and the first voltage source. The first voltage source connected to terminal 27 in Fig. 4 of Shen et al. is inherent in the disclosed circuit, since otherwise the circuit would not work. In the Baumgartner et al. device protected according to teachings of Shen et al. the diode is connected between one of the electrodes and the first voltage source. A motivation for modification of the primary reference is the same as above.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Shen, Amano and Van Kraukauer et al. (US 5,617,283). Claims 7 and 14 differ from Claims 1 and 12 rejected above by their limitations of shorting two electrodes, or drawing the current away from electrodes, thus reducing the voltage. Kraukauer et al. discloses the over-voltage protection circuit, which shortens two terminals (pad and ground, i.e. 12 and Vss in Fig. 1) in a case of the over-voltage

by activation of the protecting element (18 in Fig. 1). The protecting element (18 in Fig. 1) is drawing the current away from the couple of terminals (12 and Vss in Fig. 1) thus reducing the over-voltage between them. The reference is pertinent to the problem the inventor was solving, i.e. providing over-voltage protection to the over-voltage sensitive equipment. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the protecting element shorting the two electrodes of the protected device according to teachings of Krakauer et al., because the shorting (clamping) is the most effective way of the over-voltage protection. As Krakauer et al. stated (col. 1, lines 26 – 39), the ESD clamp shunts the current associated with an ESD event away from the operating circuit (protected device) thus maintaining the voltage at the value known to be safe for the protected device. These features make the ESD clamp preferable over other solutions such as zener diodes.

Claims 9 – 11, 18, 19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Shen, Amano and Wagner et al. (US 5,430,595). Baumgartner et al., Shen and Amano disclose all the elements of Claims 1 and 12. However, regarding Claims 9 - 11, 18, 19, they do no not disclose the voltage limiting circuit being positioned at different locations such as within a transducer probe, integrated with preamplifier, or within a transducer connector. Wagner et al. disclose the protecting diodes (elements 21, 22 in Fig. 2) being positioned adjacent to the protected elements (transistors 41, 42 in Fig. 2, col. 7, lines 3 – 19). Both references have the

same problem solving area, namely protecting the electronic circuits against over-voltages. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by placing the protecting diodes adjacent to the protected element, i.e. within a transducer probe, integrated with the preamplifier, or within a transducer connector of an imaging system (again to protect the preamplifier), because as Wagner et al. state (col. 7, lines 3 – 19), it is done to minimize the resistance between the anode of the diode and the protected element (transistor).

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is in the claim limitation of a shorting the electrodes switch being a relay, which in combination with other limitations of the claim has not been found in the collected prior art of the record.

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is in the claim limitation of shorting the first electrode to the second electrode at time other than during performance, which in combination with other limitation of the claim has not been found in the collected prior art of the record.

Response to Arguments

Applicant's Arguments have been given careful consideration but they have been found non-convincing.

1. Applicant argues that Shen et al. is not analogous art, since it allegedly is not in the same field of endeavor and is not pertinent to the problem with which Applicant's are concerned. Applicants further claim that their field of endeavor is limited to damage to ultrasound transducer flexible membranes fused in bottom-out position (page 6, last paragraph - page 7, first paragraph). According to Applicant's, Shen et al. addresses the problem of overvoltage protection of transistors, and not the flexible membranes and it is not appropriate to use any reference with overvoltage protection, which do not deal with flexible membranes.

Applicant's misrepresent the Shen et al. reference; as stated in the Office Action, the Shen et al. invention protects against over voltages the gate region of the transistor, which as well known in the art, has capacitive structure and therefore, is vulnerable to the over voltages. And as is stated in the Office Action, "The reference is pertinent to the problem soled by the inventor and has the same problem solving area, i.e. protection the capacitive structure vulnerable to ESD against over-voltages".

In response to applicant's argument that Shen et al. reference is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the

claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, (i) Examiner does not accept the argument of a field of Applicant's endeavor limited to protecting against the damage to ultrasound transducer flexible membranes fused in bottom-out position. Examiner's understanding is that the Applicant's are of expertise is in manufacturing of electronic devices, particularly the ultrasound detectors. In the Background part of Application Applicant's describe methods of overvoltage protection of piezoelectric transducers. As a matter of fact, all the Applicant's solutions are widely used for piezoelectric transducers protection. By that Applicant's demonstrated expertise in overvoltage protection of devices other than ultrasound transducer flexible membranes fused in bottom-out position.

Applicant's failed to demonstrate that the overvoltage problem in the ultrasound transducer flexible membranes has any special features requiring different approach to overvoltage protection problem than any other electronic device/circuit. As matter of fact, all the Applicant's solutions are well known and widely used in the art of protection of electronic devices. As to details of the capacitive membrane manufacturing, i.e. fused in bottom-out position, they are irrelevant to the discussed matter. (ii) As was stated above, The Shen et al. reference belongs to a problem solving area of protecting capacitive structures against overvoltages. Both the capacitive membrane and the MOS transistor gate have capacitive structure, which are vulnerable to overvoltages. Therefore, there is a common problem solving area.

2. Applicant's attack a motivation to combine Shen et al. reference with Baumgartner et al. (page 7, 2nd paragraph). Particularly, he attacks the Amano

reference used for motivational statement alleging that Amano reference is non-analogous art, since it deals with piezoelectric device rather than ultrasound transducer flexible membranes. However, as was stated above, Applicant's demonstrated their knowledge in the piezoelectric transducers (see Background section of the Application). Therefore, the piezoelectric devices cannot be considered as outside the area of Applicant's expertise. Applicants further attack the Amano reference on the basis that it discloses transducer, which is different from Applicant's structure. This is irrelevant to discussed issue, since the Amano reference used only for its motivational statement with regard to the capacitive membrane transducers; according to Amano (col. 1, lines 62 – 64), the capacitive transducers are vulnerable to the ESD and therefore, need the over-voltage protection. This statement is recited in the Background section of his Patent with reference to technologies other than his own and has nothing to do with his own invention. Therefore, criticism of Amano as a reference used only for motivational statement is pointless.

3. Regarding Claim 2 rejection, Applicant's argue the Examiner statement of inherency, alleging: "a signal trace is not inherent because a common ground plate, not a signal trance, may be connected to the electrode". However, since the discussed electrode (12 in Fig. 1) is located on the top of the flexible membrane connecting the electrode to the common ground plate without use of the signal trace, as suggested by Applicant's, requires a stretch of imagination.

4. Regarding Claim 3, Applicant attacks Shen et al. reference for not using the term "ground". According to Wikipedia, in an electrical circuit operating at signal voltages

(usually less than 50 V or so), a common return path that is the zero voltage reference level for the equipment or system. As stated in the Office Action, the term "ground" is understood as a terminal carrying a common, i.e. reference voltage. Additionally, the grounding symbol used in the Drawings indicates an analog ground, i.e. a common reference point for plurality of devices. In Baumgartner et al. system modified according to teachings of Shen et al., the zener diode is connected between the conductor and the substrate (4 in Fig. 1), which is the common return path electrode, i.e. ground.

5. Regarding Claim 5, Applicants attack the rejection for allegedly lacking the first voltage source, since the ground according to Applicant's is zero voltage source. It is true, that the ground is considered as zero voltage source. However, as stated in Claim 5 rejection, It [Shen et al.] further discloses a first couple of diodes (25 in Fig. 4) connected between the input terminal and the first voltage reference source (ground) and a second couple of diodes connected between the input terminal and the second voltage source.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
2/22/2007

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